IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2626
Examiner: Brian L. Albertalli
Confirmation No.: 4004

In Re PATENT APPLICATION Of:

Appellants:	Kiyohiko Yamazaki et al.	)	
Serial No.:	09/996,929	)	
Filed:	November 30, 2001	)	BRIEF
For:	APPARATUS INCLUDING AN ERROR DETECTOR AND A LIMITER FOR DECODING AN ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION RECEIVING SIGNAL	)	ON APPEAL
Attny Ref.:	OKI 282	)	

November 9, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is in response to the Final Official Action mailed on April 17, 2006 and follows the Amendment AFR of August 31, 2006 and the Notice of Appeal of September 15, 2006. Payment of the Brief fee is attached hereto. Please charge our Deposit Account No. 18-0002 if any other fees are needed to enter this paper, and please advise us accordingly. It is noted that no petition is required because of the authorization to charge, but this paper is a petition for extension of time.

REAL PARTY IN INTEREST

The real party in interest is Oki Electric Industry Co., Ltd., of 7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-3, 8-15, and 17-20 are pending, and claims 4-7 and 16 are canceled. Claims 1, 8, 10, and 17 are independent. All claims were rejected in the Final Official Action mailed on April 17, 2006, but claims 1-3 were allowed in the subsequent Advisory Action, so claims 8-15 and 17-20 are rejected.

STATUS OF AMENDMENTS

All amendments have been entered. The Amendment After Final Rejection of August 31, 2006 was entered according to the subsequent Advisory Action indicating that the amendment (adding "only when error occurs" at the end of claim 1) would be entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

The following features are common to all the instant claims and Figs. 1, 6, 10, and 14:

An apparatus for decoding encoded voice data comprising:

a demodulator [101, Fig. 1] *which demodulates said encoded voice data and which outputs a demodulated encoded voice data;*

an adaptive differential pulse code modulation decoder [ADPCM 102, Fig. 1] *which decodes said demodulated encoded voice data and which produces a pulse code modulation data;*

an error detector [103, Fig. 1] *which detects whether error is present in said encoded voice data and which outputs a detection result;*

....

a limiter [104 in Fig. 1].

RF. In Figs. 1, 6, 10, and 14 the input to the demodulator 101 is labeled "RF," which in electronics and in this application stands for "Radio Frequency" and refers to radio-frequency signals. Radio signals employ various "modulations" such as AM or amplitude modulation (varying the amplitude of a radio signal to encode information, such as audible sound), FM or frequency modulation (keeping the amplitude constant but varying the frequency of the radio signal), PM or phase modulation, and so on. The on/off of Morse code is also a type of modulation. The demodulator separates the encoded signal (here, voice) from the radio signal. The output of the demodulator, if suitably amplified and put into a loudspeaker, would result in intelligible speech sounds. This is an "analog" signal (page 1, line 15).

PCM. The adaptive differential pulse code modulation decoder or ADPCM, 102, of Fig. 1 takes the voice signal and re-modulates it with a variation of "pulse code modulation," invented by the digital pioneer Claude Shannon more than fifty years ago and still widely used. In this "PCM," the level of the voice signal at succeeding instants of time is encoded as digital bits.

For example, if a voltage representing the voice signal has the value 20 volts at one instant, the value of twenty is encoded as 10100, which is 20 in base 2 ($1\times16 + 0\times8 + 1\times4 + 0\times2 + 0\times1$); if one eight-thousandth of a second later the voltage representing the voice signal has the value 21 volts, then the value of twenty-one is encoded as 10101 ($1\times16 + 0\times8 + 1\times4 + 0\times2 + 1\times1$); and so every succeeding one-eight-thousandth of a second. The 1's and 0's signal (here 1010010101...) represent the original signal encoded digitally in binary notation. In an electronic device, the 1's and 0's are themselves represented by voltages, such as 1 volt and 0 volts, or sometimes by other means such as the pits and spaces in a compact disk. The output of the ADPCM, the claimed "pulse code modulation data," is a stream of 1's and 0's.

ADPCM is a variety of PCM that uses less memory to store the data (page 2, line 3).

The finer the voltage increment (one volt, i.e., 20 volts to 21 volts, in the example above) and the shorter the sampling interval (one-eight-thousandth of a second in the example above), the better the encoding (page 1, line 16). An interval of one-forty-thousandth of a second is used in CD's while cordless telephones use the interval of one eight-thousand of a second (0.000125 second) or, 8 kHz (page 1, line 19).

Error Detector. The ADPCM can have errors in it (page 2, line 7) caused by RF degradation, and this will cause audible noise in the telephone (page 2, line 11).[1] One way the prior art dealt with this problem was to cut off the telephone when the signal became too noisy; the noise was detected by looking at one particular part of the signal, which repeats at burst intervals. (The RF signal comes in bursts, as shown in Fig. 19, and some parts of each burst are the same. The burst structure is described at page 6, lines 4-20.) If this particular part of the burst, called a synchronous pattern, were not detected, then the rest of the burst was deleted. This approach led to increasing amounts of dead time as the synchronous pattern was found less and less often (page 2, lines 11-19).

According to the Appellants, "The error detector 103 detects whether the radio signal RF has a transmission error in accordance with error data in the demodulated data RD," according to the Appellants' specification at page 8, line 5, which continues, "When error is detected, the error detector 103 outputs a detection result ... CRCERR" which goes to the limiter 104 (Fig. 1). The limiter acts to reduce noise instead of simply canceling the whole signal.

The Appellants' Fig. 5 shows that the signal is modified by cutting off both low values of the signal (at 501) and also high values (at 502).

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[1] One type of noise is voltage spikes in the RF. On an AM radio, lightning causes noisy reception because it creates radio waves that add to the waves from the transmitter and are heard in the receiver. Interference can also cause noise. Loss of signal due to distance or obstacles can also create a noisy signal, because background noise becomes louder than the signal.

Limiter. Limiters of several types are shown in Figs. 2-4. As the name implies, these circuits limit the signal excursion. This feature is supported at page 8, lines 11-14 and is exemplified in Fig. 2, described on pages 9-10. The error detector's signal, detection result CRCERR, controls the logic gates 203A and 203B. The claimed upper and lower limit data are shown as upper and lower limit "values" in Fig. 2, which relates to claim 1 and Fig. 5.

The Examiner Had Misconstrued. The Examiner admitted at the personal interview that he had mistakenly taken the Appellants' Fig. 5 as showing a modulated RF signal rather than the signal itself (e.g., the input to demodulator 101 rather than the output). The Examiner therefore had taken the signal of Fig. 5 as being symmetrical about a zero value (the "central axis" asserted by the Examiner at line 6 of ¶2 on page 2), which would have made the high and low values symmetrical;[2] as a result, the Examiner took the claimed an upper limit data and lower limit data of claim 1 as being the same in amplitude. After this misunderstanding was corrected, the Examiner withdrew the rejection of claim 1.[3]

Dependent Claims 19-20. In the Amendment of January 31, 2006, at the top of page 13, the Appellant argued, "New dependent claim 19 more specifically recites two amplitudes of signal, and more clearly distinguishes over Murata, as does new claim 20." However, the Examiner apparently did not consider this further argument, and now rejects these claims in spite of the fact that they depend from allowed claim 1. Claims 19 and 20 are supported at page 9, lines 3-6 and page 10, line 20, respectively.

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[2] The Examiner states this in the first paragraph on page 3 of the Final Action.

[3] The Appellants noted on page 9 of the August 31, 2006 Amendment After Final Rejection that "the presently-requested amendment at the end of claim 1, which was suggested by the Examiner at the interview, is unrelated to any outstanding rejection. It addresses a concern of the Examiner which is not of record and was first mentioned to the Appellants on August 22, 2006. Therefore, the Appellants could not have been expected to make this amendment earlier, i.e., prior to the final rejection."

Claim 8. Claim 8 also recites a limiter but not the fixed upper limit data and lower limit data of claim 1. Instead, claim 8 recites a *variable* upper limit and lower limit. The honorable Board is referred to the Appellants' Fig. 6. Claim 8, as exemplified in Figs. 6-7, reads:

a threshold value setting portion [601] *which calculates a limit data* [THV] *based on said pulse code modulation data* [PO] *and which outputs said limit data* [THV] , *wherein the threshold value setting portion comprises:*

an average calculating portion [701, Fig. 7, and page 17, line 13] *which calculates an average value of a numerical value data of said pulse code modulation data* [PO] *and which outputs said average value* [page 17, lines 6-10]*;*

a latch portion [702] *which latches said average value and which outputs said stored average value* [page 18, line 14] *based on a voltage level of a control signal* [DLT]*; and*

a limiter [104, Fig. 6] *which outputs either said pulse code modulation data* [PO] *or said limit data* [THV] *in accordance with said detection result* [page 18, lines 14-19].

The action of this embodiment is illustrated in Fig. 9 and explained on page 19. At first (on the left in Fig. 9), the signal (the wavy line) stays between upper limit and lower thresholds or limits (horizontal lines) and the limiter merely passes this voice signal through (page 19, lines 6-11). The upper limit and the lower thresholds are based on average values calculated by the average calculating portion 701 (page 18, line 16).

At point 901 the signal drops below the lower thresholds (page 19, line 12) and the limiter keeps the signal within the limits (page 19, line 13).

When the signal amplitude decreases (between points 901 and 902), the thresholds, which are based on the average signal as calculated by the average calculating portion 701, change. Then at point 902 there is a second excursion and again the output is limited but this time to the

new threshold (page 20, line 7). This embodiment has the advantage that the limitation is scaled to the signal (top of page 21).

The threshold Value Setting Portion is also recited in independent claims 10 and 17.

The Board is invited to note that the average calculated by the average calculating portion 701 is an average of the data, not an average of the voltage that carries the data. The data, when in PCM format, is embodied in two voltages corresponding to "0" and "1" binary digits. If these two voltages are zero volts and one volt, then the average voltage is one half; but this is not the average of the data that is encoded in binary format.

The specification on page 18, lines 6-13 describes how a sum (ACCO) is divided by an integer N. This result is stored in a latch 702, which is a device for holding a set of bits or digital values. The average is stored as a binary number.

Claim 17. Fig. 10 illustrates one feature not seen in Fig. 6, namely, the error signal CRCEER going to the threshold value setting portion 1001 as well as to the limiter 104. This feature is recited in independent claim 17, which is similar to claim 8 except that in the 5th paragraph it recites a threshold value setting portion which calculates limit data based on "said pulse code modulation data produced at a term and which outputs said limit data, wherein said term is a term that a transmission error is not present in said encoded voice signal." Fig. 11 shows how the signal CRCERR controls the latch 1102B.

Claim 10. Claim 10, as exemplified in Fig. 14, reads:

a threshold value setting portion [601] *which calculates a limit data based on said pulse code modulation data* [PO] *and which outputs said limit data* [THV];

a counter [1401] *which counts the number of times that said pulse code modulation data* [PO] *is over said limit data and which outputs a count result having a voltage level when said count result is over a predetermined value; and*

a limiter [1402] *which outputs either said pulse code modulation data* [PO] *or said limit data* [THV] *in accordance with said* [error] *detection result* [CRCERR] *, and which outputs the selected data in accordance with said count result.*

This fourth embodiment is described in the specification starting at page 26, line 3. The counting by the counter 1401 is described at page 26, line 20.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claim 10 was rejected under §112 under §112, second paragraph.

Claim 19 is rejected under §102 over Murata '146.

Claims 8, 17, and 18 were rejected under §103 over Murata in view of Butcher '863.

Claim 9 was rejected under §103 over Murata and Butcher in view of Official Notice.

Claims 10-15 and 20 were rejected under §103 over Murata in view of Wiatrowski '941.

ARGUMENT: §112

Claim 10 recites "a limiter which outputs either said pulse code modulation data or said limit data in accordance with said detection result, and which outputs the selected data in accordance with said count result." The Appellants believe that "selected" clearly refers to one of the two types of data which are output, and therefore meets the requirements of §112. However, the Examiner is authorized to change "the selected data" to "either said pulse code modulation data or said limit data" in order to simplify the issues.

ARGUMENT: CLAIM 19

Claim 19 is allowable by being dependent from allowed claim 1.

ARGUMENT: CLAIM 20

Claim 20 is allowable by being dependent from allowed claim 1.

ARGUMENT: CLAIMS 8 AND 17

Claims 8 and 17 recite a threshold value setting portion having *an average calculating portion which calculates an average value of a numerical value data of said pulse code modulation data and which outputs said average value.* On page 14 of the final Action, the Examiner admits that Murata does not disclose this but asserts that Butcher discloses this feature at col. 3, lines 1-8, which reads, "the bias circuit is set to rapidly adjust the reference threshold in the limiter circuit to the average voltage of the incoming signal."

DC Offset. At col. 3, line 3, the cited passage refers to "variations in the DC offset voltage in a received data signal." The honorable Board will note that this offset voltage is also mentioned at col. 1, line 33 ("DC" does not appear there, but any steady voltage is a "DC" voltage) and it is related to the "1-0 information" mentioned at col. 1, line 29.

The "1-0 information" consists of digital 1s and 0s. The short-term DC average of such a digital signal will vary depending on the proportion of digital 1s and 0s, because the two digital values are represented by two different voltages (for example, "0" may be represented by 0 volts and "1" by 0.9 volts). If there is a long string of 0s the short-term average voltage will approach the "0" voltage, and differ from short-term average voltage due to a long string of 1s and also from the intermediate voltage resulting from the usual equal mix of 1s and 0s.

Butcher says (col. 1, line 38), "However, once a word synch signal has been detected, the bias level [DC offset] must not vary [even with] long strings of consecutive 'ones' or 'zeros'." The applied passage at col. 3, lines 1-8, states, "in an idle state, the data decoder circuit 20 will set the fast recovery bias circuit 16 to respond to rapid variations in the DC offset voltage ... the bias circuit is set to rapidly adjust ... to the average value of the incoming data signal." Then, at the following line 9, Butcher writes, "After word synch has been detected, the data decoder sets the fast recovery bias circuit to prevent ... changes ... to the DC offset."

Fig. 2 shows the circuit which does this (col. 3, line 16). It is an "RC" (resistor-capacitor) circuit which acts as a "low-pass filter" (col. 3, line 38). Before the word synch is detected, it passes below signals 50 Hz; after, it passes signals below 5 Hz (col. 3, lines 39 and 52).

Butcher Does Not Anticipate. Butcher does not anticipate for the following reasons:

(1) Although the reference says that it finds an average, it does not. An RC circuit is actually an *integrating* circuit in which the capacitor rises to the maximum applied voltage in a short time, the time depending on the values of resistance R and capacitance C. If Fig. 2 of Butcher the capacitor 32 has no way to discharge except through the comparator 34, and that, being an amplifier (this is disclosed by the shape), probably has high impedance inputs. Therefore, the capacitor 32 will charge to the maximum voltage (e.g., the high voltage corresponding to digit "1") and stay there. Then, when the voltage drops during a "0" signal, the capacitor 32 will be at the high voltage and the signal line at the low voltage. The comparator 34 then puts out a signal like the original because of this difference (the honorable Board is invited to note the - and + signs on the comparator inputs). The switching between 50 Hz and 5 Hz that is discussed by Butcher relates to how fast the capacitor 32 can react to a shift in the voltages corresponding to "0" and "1" and not to the average of the voltages. There is no average voltage in the circuit of Fig. 2.

(2) Butcher does not "output" an average because there is no average. As to the voltage in the capacitor 32, it is not output either. The only output is from the comparator 34, and that output is not an average or the voltage in the capacitor 32, it is the signal itself.

The outgoing signal very likely has the DC offset removed. The output from the comparator 34 is proportional to the voltage *difference* between the average voltage at the lower end of capacitor 30 and the original signal at the upper end of capacitor 30.

(3) Butcher does not disclose "*calculating* a *numerical* average value" because it does not calculate, it filters or integrates; and the voltage averages is not a *numerical* average, it is just a

voltage. As discussed above, the Appellant stores its average in a latch as digital (numerical) data of several bits; Butcher does nothing of the kind.

(4) Butcher also does not disclose an average of a numerical value data of *pulse code modulation data*. Instead, it discloses a summation of voltages of bits. While bits 1100 sum to 2 and bits 1001 sum to two, 1100 is not equal to 1001 .

Combination. The combination of Murata and Butcher is respectfully traversed. The Examiner asserts that it would have been obvious to use an average instead of a maximal value in the clipping circuit of Murata, but the Appellants believe that a clipping circuit which clipped everything above the average value would have no output at all. The Examiner is invited to consider Fig. 25 of Murata, where the average value is indicated by a dashed line in the middle of the signal.

ARGUMENT: CLAIM 9

The Examiner asserts (¶4 on page 7 of the final Action) that the Appellants are estopped from traversing official notice and cites MPEP §2144.03. However, the Examiner does not cite within that section of the MPEP, and the Appellants see nothing about estoppel in §2144.03. The Appellants did not previously traverse the Examiner's official notice because they did not specifically traverse the rejection of claim 9, which is dependent. The assertion that the Appellants are estopped is respectfully traversed.

The Appellants now traverse and request that the Examiner cite a reference showing an average calculated with an accumulator which adds pulse code modulation numerical data and a stored value, and replaces the stored value with the addition result, with multiplication of the addition result and a coefficient; which is the Examiner asserts is notoriously well-known.

ARGUMENT: CLAIM 10

Claim 10 recites *a counter which counts the number of times that said pulse code modulation data is over said limit data and which outputs a count result having a voltage level when said count result is over a predetermined value.* The Examiner at pages 18-19 of the Action admits that Murata does not disclose this but asserts that Wiatrowski discloses a counter which counts the number of times that pulse code modulation data is over a limit. The Appellants respectfully disagree.

Wiatrowski writes (col. 4, line 54), "Each time [a measurement] is above the upper threshold, that threshold is increased. Each time a [measurement] is below the upper threshold, a value called a symbol count is increased by one." Thus, counting only takes place when the measurement is *under* the threshold, not *over* as the Appellants' claim recites; when it is over, the threshold is altered.

The threshold is changed depending on the "symbol count." This count is increased by one until the symbol count reaches seven, after which the upper threshold is decreased and the symbol count is reset (col. 4, lines 58-66). Thus, Wiatrowski does not disclose counting the number of times that the pulse code modulation data is over a limit, it counts the number of times it is under a limit. The reference also fails to disclose *output*[ing] *a count result having a voltage level when said count result is over a predetermined value.* Instead, when the a predetermined value (seven) is reached, it resets rather than outputting a voltage.

The Examiner asserts that combination would have been obvious to count the number of times Murata's signal went over a limit, so that a single high value would not set the threshold too high. The Appellants respectfully disagree. There is nothing on the record to indicate that a single high value would affect the threshold of Murata, which appears to clip anything over the clip value 114, regardless of amplitude.

For the reasons above, the honorable Board is requested to overturn the rejections.

Respectfully submitted,

November 7, 2006
Date

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CLAIMS APPENDIX

1. (previously presented): An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data;

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result; and

a limiter which outputs said pulse code modulation data when the pulse code modulation data is within a range from an upper limit data to a lower limit data, outputs the upper limit data when the pulse code modulation data is greater than the upper limit data, and outputs the lower limit data when the pulse code modulation data is lower than the lower limit data, only when error occurs.

2. (previously presented): The apparatus for decoding encoded voice data according to claim 1, further comprising:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result;

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result; and

a first output portion which outputs said pulse code modulation data, said upper limit data or said lower limit data in accordance with said detection result and said first and second comparison results.

3. (previously presented): The apparatus for decoding encoded voice data according to claim 2, wherein said first output portion comprises:

a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level;

a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level; and

a selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, selects said lower limit data when said second logic circuit result having said first voltage level is input, or selects said pulse code modulation data when said first and second logic circuit results, each not having said first voltage level, is input.

4.-7. (canceled)

8. (previously presented): An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data:

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

an error detector which detects whether an error is present in said encoded voice data and which outputs a detection result;

a threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data, wherein the threshold value setting portion comprises:

an average calculating portion which calculates an average value of a numerical value data of said pulse code modulation data and which outputs said average value;

a latch portion which latches said average value and which outputs said stored average value based on a voltage level of a control signal; and

a limiter which outputs either said pulse code modulation data or said limit data in accordance with said detection result.

9. (previously presented): The apparatus for decoding encoded voice data according to claim 8, wherein said average calculating portion comprises:

an accumulator which executes an addition of said numerical value data of said pulse code modulation data and a stored value, which replaces said stored value with an addition result, and which outputs said addition result; and

a multiple portion which executes a multiple operation of said addition result and a coefficient.

10. (previously presented): An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data:

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data;

an error detector which detects whether an error is present in said encoded voice data and which outputs a detection result;

a threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data;

a counter which counts the number of times that said pulse code modulation data is over said limit data and which outputs a count result having a voltage level when said count result is over a predetermined value; and

a limiter which outputs either said pulse code modulation data or said limit data in accordance with said detection result, and which outputs the selected data in accordance with said count result.

11. (previously presented): The apparatus for decoding encoded voice data according to claim 10, wherein said limit data has an upper limit data and a lower limit data; and wherein said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result;

a second comparator which compares said pulse code modulation data and said lower limit value and which outputs a second comparison result; and

an output portion which does not output said pulse code modulation data when said count result is input having said voltage level.

12. (previously presented): The apparatus for decoding encoded voice data according to claim 11, wherein said output portion comprises:

a first logic circuit which outputs a first logic circuit result having said voltage level when both a voltage level of said first comparison result and of said detection result are said voltage level;

a second logic circuit which outputs a second logic circuit result having said voltage level when both a voltage level of said second comparison result and of said detection result are said voltage level;

a first selector which selects said upper limit data when said first logic circuit result having said voltage level is input, selects said lower limit data when said second logic circuit result having said voltage level is input, or selects said pulse code modulation data when said first and second logic circuit results, each not having said voltage level, is input; and

a controller which does not output said data output by said first selector when said count result is input having said voltage level.

13. (previously presented): The apparatus for decoding encoded voice data according to claim 10, wherein a format of said limit data is the absolute value; and wherein said limiter portion comprises:

a comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a comparison result; and

an output portion which does not output said pulse code modulation data or said limit data when said count result is input having said voltage level.

14. (previously presented): The apparatus for decoding encoded voice data according to claim 13, wherein said output portion comprises:

a logic circuit which outputs a logic circuit result having said voltage level when both a voltage level of said comparison result and of said detection result are said voltage level;

a selector which selects said limit data when said logic circuit result having said voltage level is input or said numerical value data when said logic circuit result having said voltage level is not input;

a combiner which combines a code data of said pulse code modulation data and said data selected by said selector and which outputs a combined data; and

a controller which does not output said combined data output by said combiner when said count result is input having said voltage level.

15. (previously presented): The apparatus for decoding encoded voice data according to claim 13, wherein said output portion comprises:

a logic circuit which outputs a logic circuit result having said voltage level when both a voltage level of said comparison result and of said detection result are said voltage level;

a combiner which combines a code data of said pulse code modulation data and said limit data and which outputs a combined limit data; and

a selector which does not select said combined limit data and said pulse code modulation when said count result is input having said voltage level.

16. (canceled)

17. (previously presented): An apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data;

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces pulse code modulation data;

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result;

a threshold value setting portion which calculates limit data based on said pulse code modulation data produced at a term and which outputs said limit data, wherein said term is a term that a transmission error is not present in said encoded voice signal, and wherein the threshold value setting portion comprises:

an average calculating portion which calculates an average value of a numerical value data of said pulse code modulation data and which outputs said average value;

an output portion which stores said average value based on the voltage levels of a control signal and said detection result and which outputs a stored average value as said limit data; and

a limiter which outputs either said pulse code modulation data or said limit data in accordance with said detection result.

18. (previously presented): The apparatus for decoding encoded voice data according to claim 17, wherein said output portion comprises:

a logic circuit which outputs a logic circuit result having a first voltage level when a voltage level of said control signal is said first voltage level and when a voltage level of said detection result is a second voltage level; and

a latch portion which stores said average value based on a voltage level of said logic circuit result and which outputs a stored average value.

19. (previously presented): The apparatus for decoding encoded voice data according to claim 1, wherein the upper limit value is a largest amplitude value of a voice signal at which the reproduced voice signal does not have noise, and the lower limit value is the smallest amplitude value of a voice signal at which the reproduced voice signal does not have noise.

20. (previously presented): The apparatus for decoding encoded voice data according to claim 1, wherein the upper limit value and the lower limit value are set individually and freely.

EVIDENCE APPENDIX

There is no evidence to submit.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.